TPA6111A2 150-mW Stereo Audio Power Amplifier

1 Features

- 150-mW Stereo Output
- PC Power Supply Compatible
  - Fully Specified for 3.3-V and 5-V Operation
  - Operation to 2.5 V
- Pop Reduction Circuitry
- Internal Midrail Generation
- Thermal and Short-Circuit Protection
- Surface-Mount Packaging
  - PowerPAD™ MSOP
  - SOIC
- Pin Compatible With TPA122, LM4880, and LM4881 (SOIC)

2 Applications

- Smart Phones and Wireless Handsets
- Portable Tablets
- Notebook PCs and Docking Stations

3 Description

The TPA6111A2 is a stereo audio power amplifier packaged in either an 8-pin SOIC or an 8-pin PowerPAD MSOP package capable of delivering 150 mW of continuous RMS power per channel into 16-Ω loads. Amplifier gain is externally configured by means of two resistors per input channel and does not require external compensation for settings of 0 to 20 dB.

THD+N, when driving a 16-Ω load from 5 V, is 0.03% at 1 kHz, and less than 1% across the audio band of 20 Hz to 20 kHz. For 32-Ω loads, the THD+N is reduced to less than 0.02% at 1 kHz, and is less than 1% across the audio band of 20 Hz to 20 kHz. For 10-kΩ loads, the THD+N performance is 0.005% at 1 kHz, and less than 0.5% across the audio band of 20 Hz to 20 kHz.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPA6111A2	SOIC (8)	4.90 mm × 3.91 mm
	MSOP (8)	3.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application Circuit

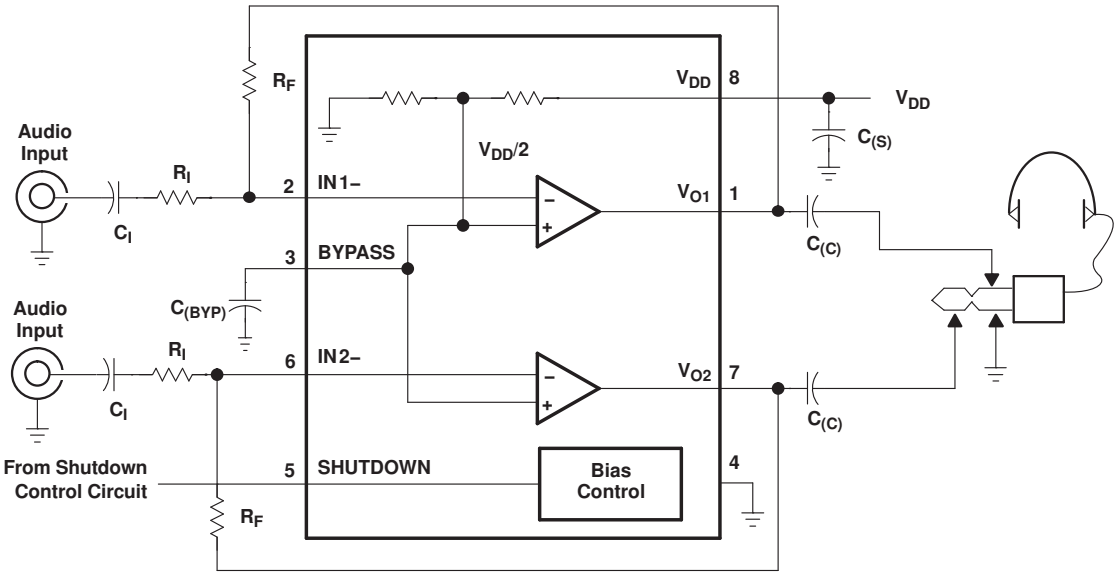


Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

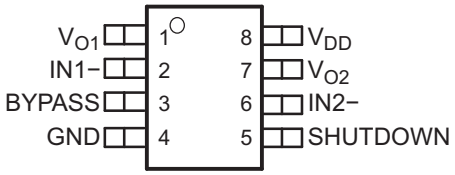
Changes from Revision B (June 2014) to Revision C	Page
• Added *Device Comparison* table, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1
• Removed *Dissipation Ratings* table	1

5 Device Comparison Table

AVAILABLE OPTIONS	TPA6100A2	TPA6110A2	TPA6111A2	TPA6112A2
Headphone Channels	Stereo	Stereo	Stereo	Stereo
Output Power (W)	0.05	0.15	0.15	0.15
PSRR (dB)	72	83	83	83
Pin/Package	8-pin SOIC, 8-Pin VSSOP	8-pin MSOP	8-pin MSOP, 8-Pin SOIC	10-pin MSOP

6 Pin Configuration and Functions

D or DGN Package
8-Pin SOIC or MSOP
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
BYPASS	3	I	Tap to voltage divider for internal mid-supply bias supply. Connect to a 0.1-µF to 1-µF low ESR capacitor for best performance.
GND	4	I	GND is the ground connection.
IN1–	2	I	IN1– is the inverting input for channel 1.
IN2–	6	I	IN2– is the inverting input for channel 2.
SHUTDOWN	5	I	Puts the device in a low quiescent current mode when held high
V_{DD}	8	I	V_{DD} is the supply voltage terminal.
V_{O1}	1	O	V_{O1} is the audio output for channel 1.
V_{O2}	7	O	V_{O2} is the audio output for channel 2.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
V_{DD}	Supply voltage		6	V
V_I	Input voltage	–0.3	V_{DD} + 0.3	V
	Continuous total power dissipation	Internally Limited		
T_J	Operating junction temperature	–40	150	°C
	Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds		260	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

		MIN	MAX	UNIT
V_{DD}	Supply voltage	2.5	5.5	V
T_A	Operating free-air temperature	–40	85	°C
V_{IH}	High-level input voltage (SHUTDOWN)	60% × V_{DD}		V
V_{IL}	Low-level input voltage (SHUTDOWN)		25% × V_{DD}	V

7.4 Thermal Information

THERMAL METRIC (1)		TPA6111A2		UNIT
		D (SOIC)	DGN (MSOP)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	114.7	55.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	59.0	47.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	54.9	36.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	14.2	2.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	54.4	36.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	9.2	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

7.5 DC Electrical Characteristics, V_{DD} = 3.3 V

at V_{DD} = 3.3 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OO}	Output offset voltage				10	mV
PSRR	Power supply rejection ratio	V_{DD} = 3.2 V to 3.4 V		70		dB
I_{DD}	Supply current	SHUTDOWN (pin 5) = 0 V		1.5	3	mA
$I_{DD(SD)}$	Supply current in shutdown mode	SHUTDOWN (pin 5) = V_{DD}		1	10	µA
Z_i	Input impedance			> 1		MΩ

7.6 AC Operating Characteristics, V_{DD} = 3.3 V

V_{DD} = 3.3 V, T_A = 25°C, R_L = 16 Ω

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_O	Output power (each channel)	THD ≤ 0.1%, f = 1 kHz		60		mW
THD+N	Total harmonic distortion + noise	P_O = 40 mW, 20 Hz – 20 kHz		0.4%		
B_{OM}	Maximum output power BW	G = 20 dB, THD < 5%		> 20		kHz
	Phase margin	Open-loop		96°		
	Supply ripple rejection	f = 1 kHz, $C_{(BYP)}$ = 0.47 µF		71		dB
	Channel/channel output separation	f = 1 kHz, P_O = 40 mW		89		dB
SNR	Signal-to-noise ratio	P_O = 50 mW, A_V = 1		100		dB
V_n	Noise output voltage	A_V = 1		11		µV(rms)

7.7 DC Electrical Characteristics, V_{DD} = 5.5 V

at V_{DD} = 5.5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OO}	Output offset voltage				10	mV
PSRR	Power supply rejection ratio	V_{DD} = 4.9 V to 5.1 V		70		dB
I_{DD}	Supply current	SHUTDOWN (pin 5) = 0 V		1.6	3.2	mA
$I_{DD(SD)}$	Supply current in shutdown mode	SHUTDOWN (pin 5) = V_{DD}		1	10	µA
$\|I_{IH}\|$	High-level input current (SHUTDOWN)	V_{DD} = 5.5 V, V_I = V_{DD}			1	µA
$\|I_{IL}\|$	Low-level input current (SHUTDOWN)	V_{DD} = 5.5 V, V_I = 0 V			1	µA
Z_i	Input impedance			> 1		MΩ

7.8 AC Operating Characteristics, V_{DD} = 5.5 V

V_{DD} = 5 V, T_A = 25°C, R_L = 6 Ω

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_O	Output power (each channel)	THD ≤ 0.1%, f = 1 kHz		150		mW
THD+N	Total harmonic distortion + noise	P_O = 100 mW, 20 Hz – 20 kHz		0.6%		
B_{OM}	Maximum output power BW	G = 20 dB, THD < 5%		> 20		kHz
	Phase margin	Open-loop		96°		
	Supply ripple rejection ratio	f = 1 kHz, $C_{(BYP)}$ = 0.47 µF		61		dB
	Channel/channel output separation	f = 1 kHz, P_O = 100 mW		90		dB
SNR	Signal-to-noise ratio	P_O = 100 mW, A_V = 1		100		dB
V_n	Noise output voltage	A_V = 1		11.7		µV(rms)

7.9 AC Operating Characteristics, V_{DD} = 3.3 V

V_{DD} = 3.3 V, T_A = 25°C, R_L = 32 Ω

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_O	Output power (each channel)	THD ≤ 0.1%, f = 1 kHz		35		mW
THD+N	Total harmonic distortion + noise	P_O = 40 mW, 20 Hz – 20 kHz		0.4%		
B_{OM}	Maximum output power BW	G = 20 dB, THD < 2%		> 20		kHz
	Phase margin	Open-loop		96°		
	Supply ripple rejection	f = 1 kHz, $C_{(BYP)}$ = 0.47 µF		71		dB
	Channel/channel output separation	f = 1 kHz, P_O = 25 mW		75		dB
SNR	Signal-to-noise ratio	P_O = 90 mW, A_V = 1		100		dB
V_n	Noise output voltage	A_V = 1		11		µV(rms)

7.10 AC Operating Characteristics, V_{DD} = 5 V

V_{DD} = 5 V, T_A = 25°C, R_L = 32 Ω

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_O	Output power (each channel)	THD ≤ 0.1%, f = 1 kHz		90		mW
THD+N	Total harmonic distortion + noise	P_O = 20 mW, 20 Hz – 20 kHz		2%		
B_{OM}	Maximum output power BW	G = 20 dB, THD < 2%		> 20		kHz
	Phase margin	Open-loop		97°		
	Supply ripple rejection	f = 1 kHz, $C_{(BYP)}$ = 0.47 µF		61		dB
	Channel/channel output separation	f = 1 kHz, P_O = 65 mW		98		dB
SNR	Signal-to-noise ratio	P_O = 90 mW, A_V = 1		104		dB
V_n	Noise output voltage	A_V = 1		11.7		µV(rms)

7.11 Typical Characteristics

Table 1. Table of Graphs

			FIGURE
THD+N	Total harmonic distortion + noise	vs Frequency	Figure 1, Figure 3, Figure 5, Figure 6, Figure 7, Figure 9, Figure 11, Figure 13
		vs Output power	Figure 2, Figure 4, Figure 8, Figure 10, Figure 12, Figure 14
	Supply ripple rejection ratio	vs Frequency	Figure 15, Figure 16
V_n	Output noise voltage	vs Frequency	Figure 17, Figure 18
	Crosstalk	vs Frequency	Figure 19-Figure 24
	Shutdown attenuation	vs Frequency	Figure 25, Figure 26
	Open-loop gain and phase margin	vs Frequency	Figure 27, Figure 28
	Output power	vs Load resistance	Figure 29, Figure 30
I_{DD}	Supply current	vs Supply voltage	Figure 31
SNR	Signal-to-noise ratio	vs Voltage gain	Figure 32
	Power dissipation and amplifier	vs Load power	Figure 33, Figure 34

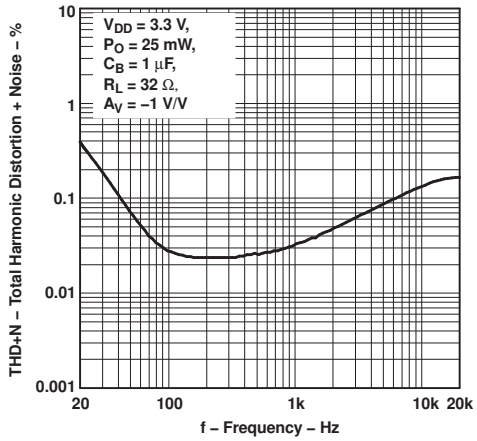


Figure 1. Total Harmonic Distortion + Noise vs Frequency

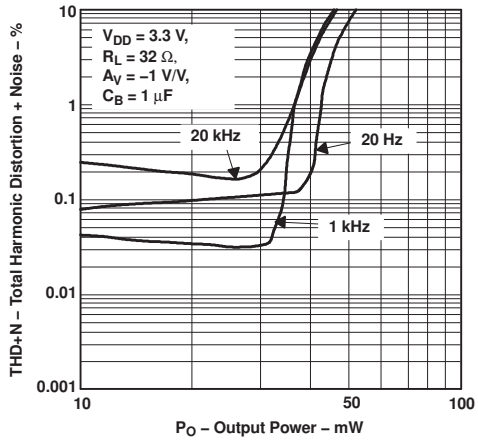


Figure 2. Total Harmonic Distortion + Noise vs Output Power

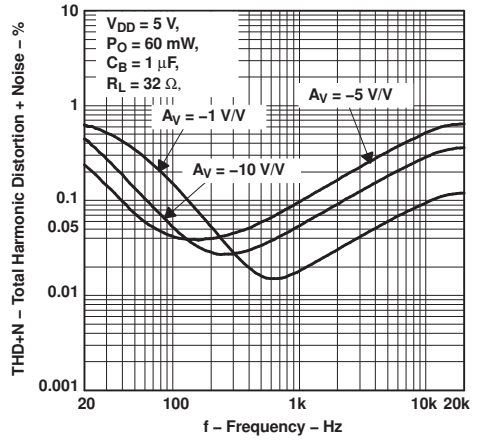


Figure 3. Total Harmonic Distortion + Noise vs Frequency

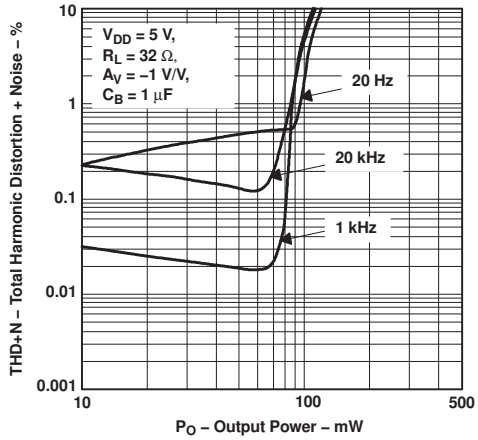


Figure 4. Total Harmonic Distortion + Noise vs Output Power

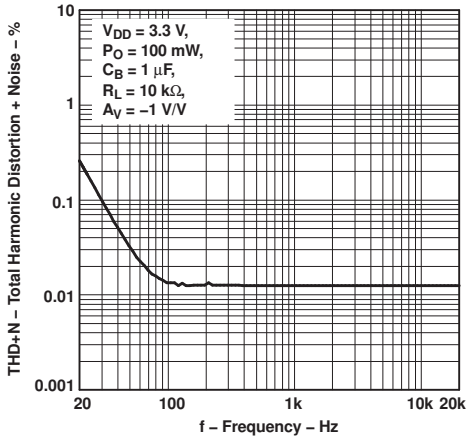


Figure 5. Total Harmonic Distortion + Noise vs Frequency

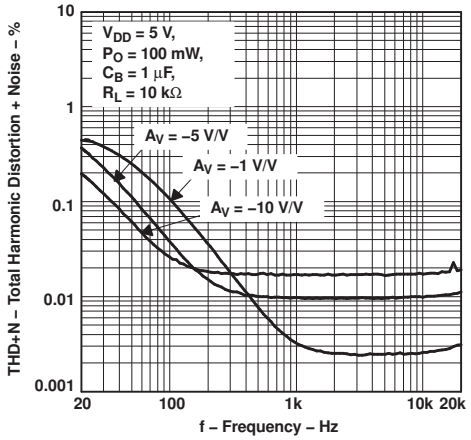


Figure 6. Total Harmonic Distortion + Noise vs Frequency

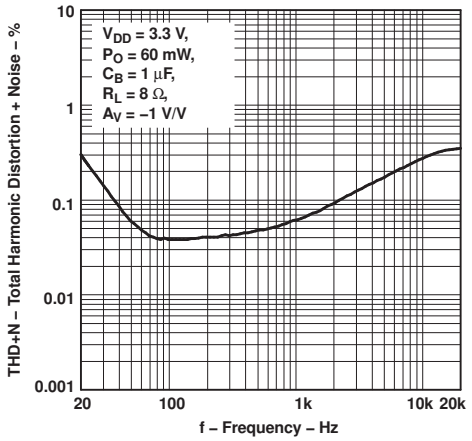


Figure 7. Total Harmonic Distortion + Noise vs Frequency

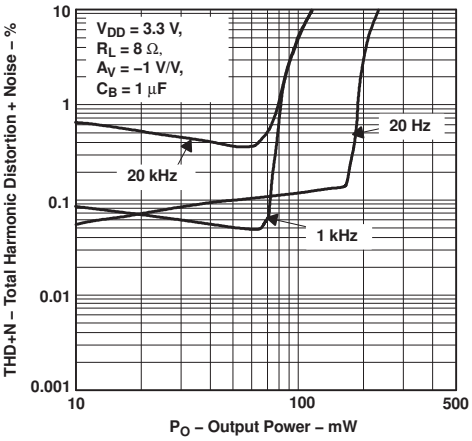


Figure 8. Total Harmonic Distortion + Noise vs Output Power

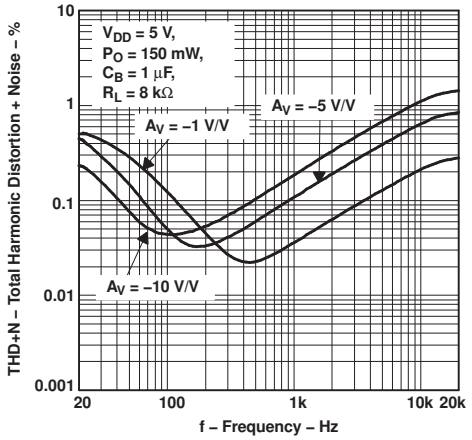


Figure 9. Total Harmonic Distortion + Noise vs Frequency

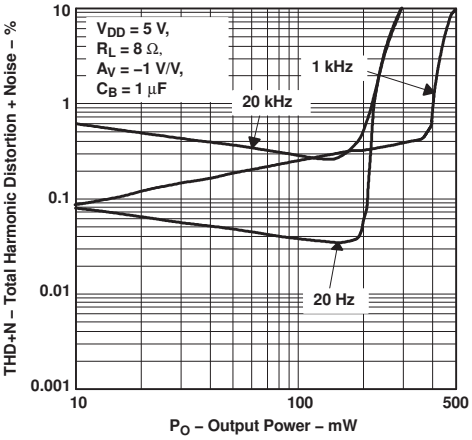


Figure 10. Total Harmonic Distortion + Noise vs Output Power

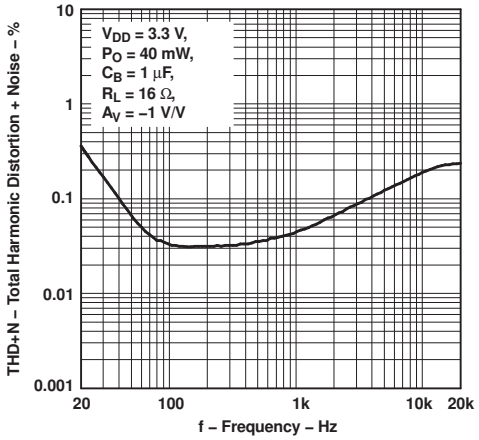


Figure 11. Total Harmonic Distortion + Noise vs Frequency

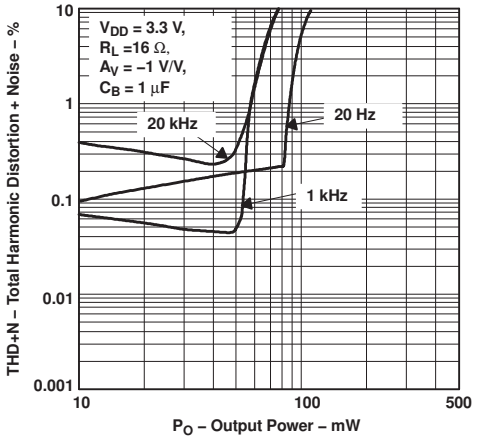


Figure 12. Total Harmonic Distortion + Noise vs Output Power

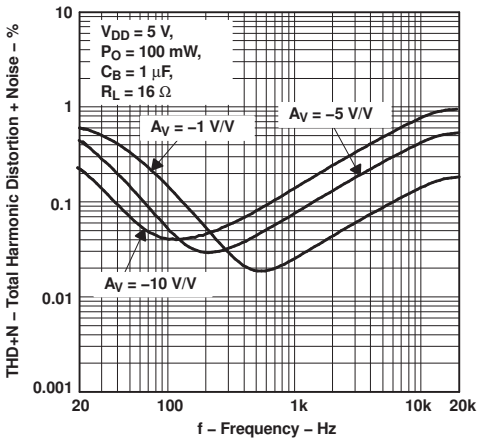


Figure 13. Total Harmonic Distortion + Noise vs Frequency

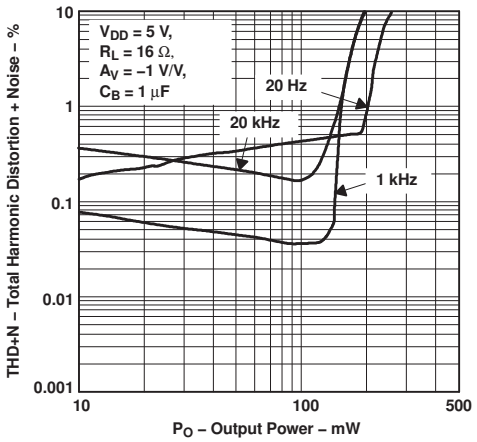


Figure 14. Total Harmonic Distortion + Noise vs Output Power

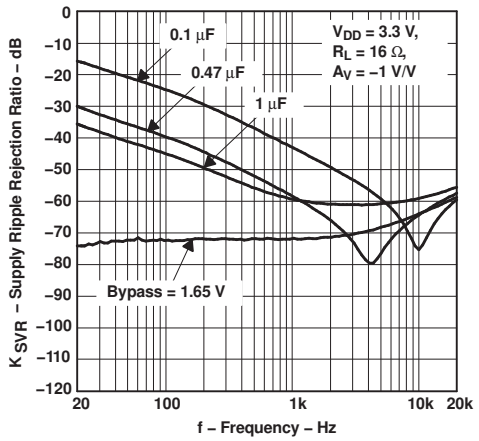


Figure 15. Supply Ripple Rejection Ratio vs Frequency

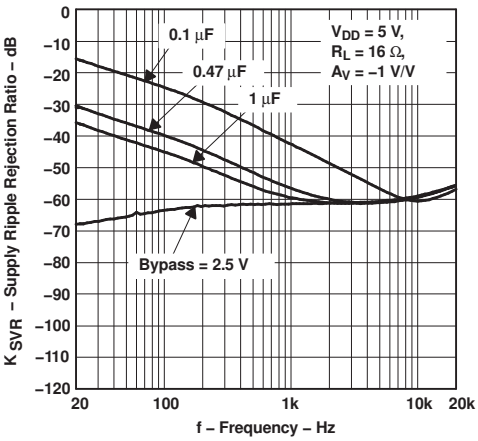


Figure 16. Supply Ripple Rejection Ratio vs Frequency

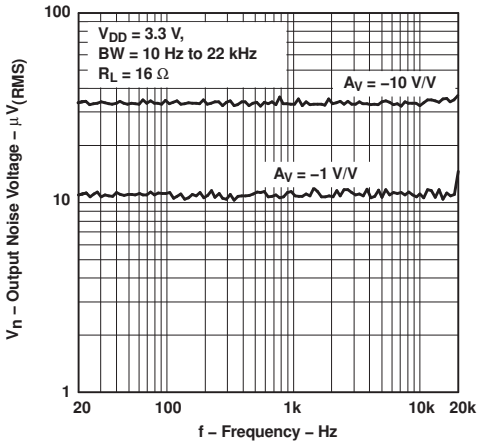


Figure 17. Output Noise Voltage vs Frequency

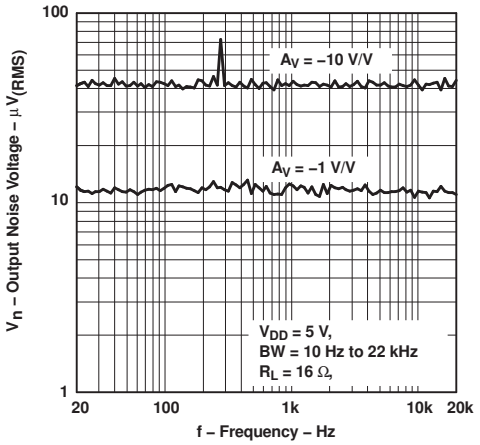


Figure 18. Output Noise Voltage vs Frequency

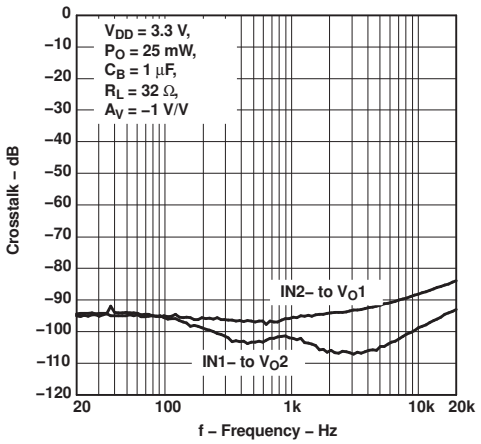


Figure 19. Crosstalk vs Frequency

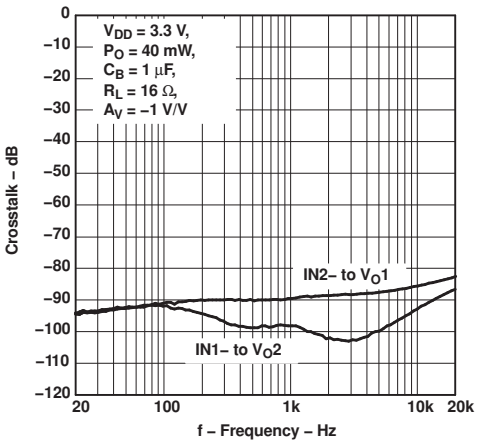


Figure 20. Crosstalk vs Frequency

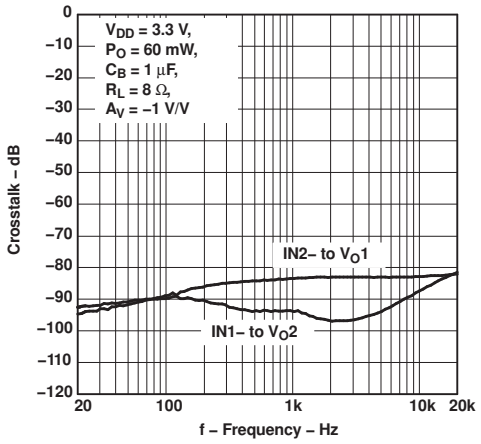


Figure 21. Crosstalk vs Frequency

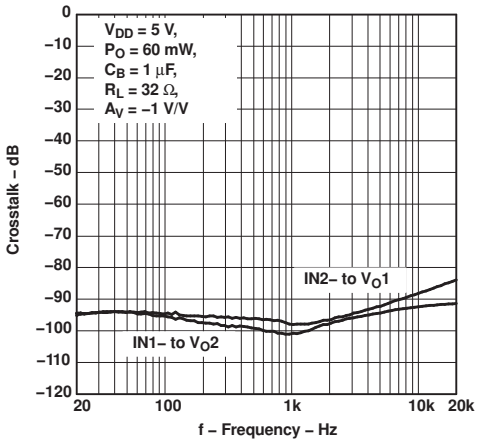


Figure 22. Crosstalk vs Frequency

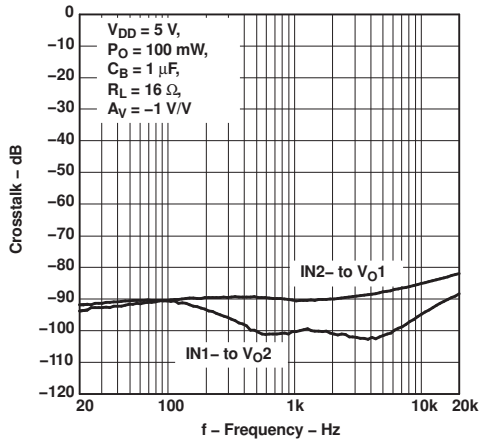


Figure 23. Crosstalk vs Frequency

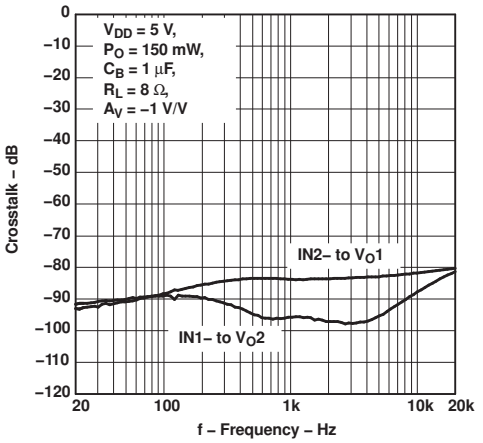


Figure 24. Crosstalk vs Frequency

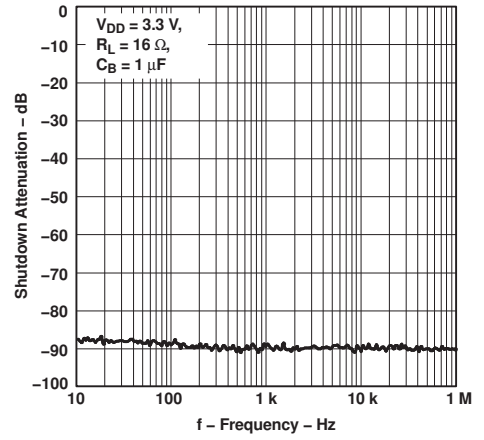


Figure 25. Shutdown Attenuation vs Frequency

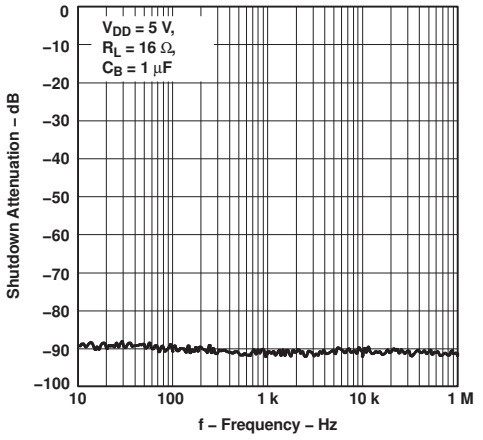


Figure 26. Shutdown Attenuation vs Frequency

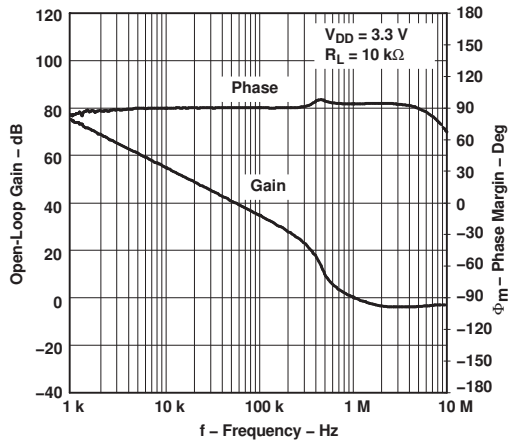


Figure 27. Open-Loop Gain and Phase Margin vs Frequency

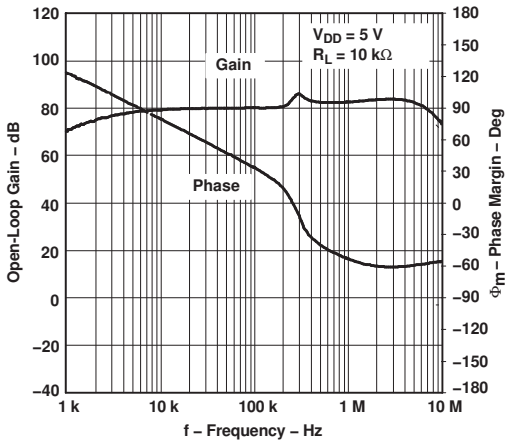


Figure 28. Open-Loop Gain and Phase Margin vs Frequency

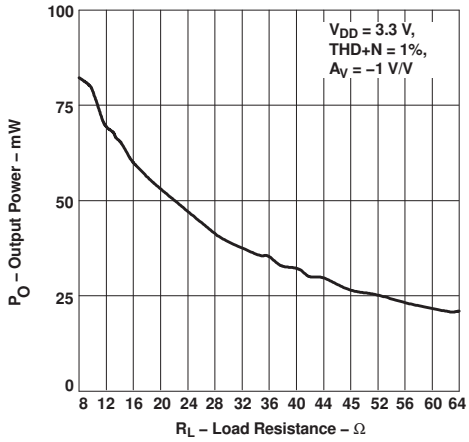


Figure 29. Output Power vs Load Resistance

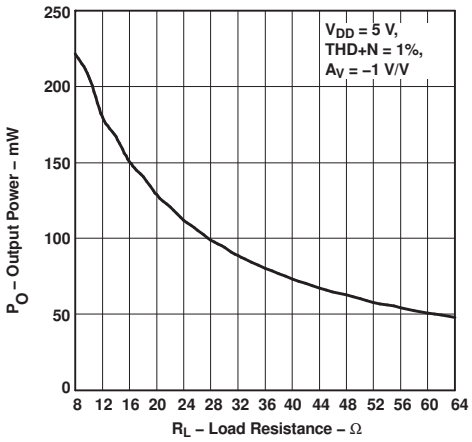


Figure 30. Output Power vs Load Resistance

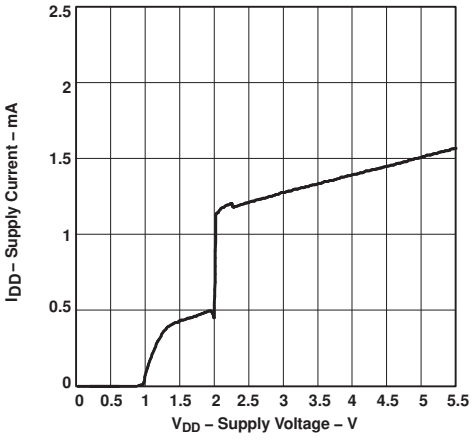


Figure 31. Supply Current vs Supply Voltage

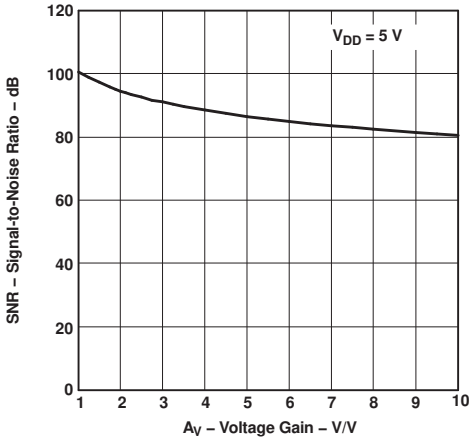


Figure 32. Signal-to-Noise Ratio vs Voltage Gain

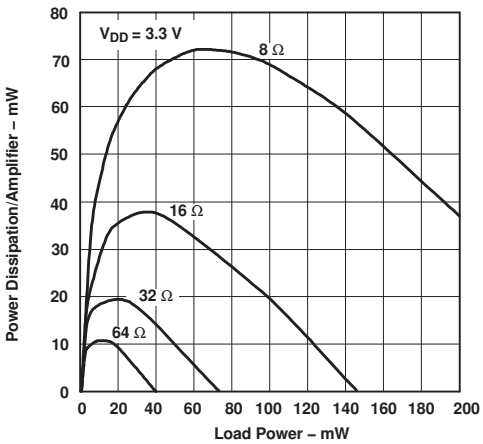


Figure 33. Power Dissipation and Amplifier vs Load Power

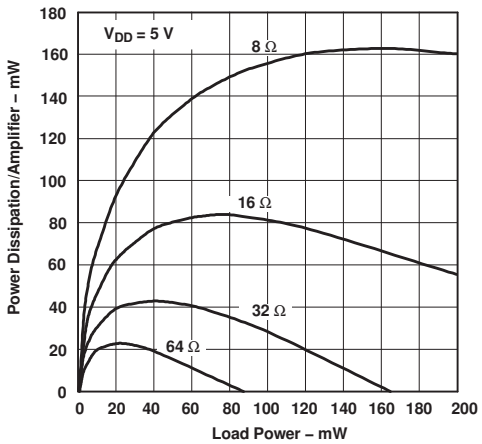


Figure 34. Power Dissipation and Amplifier vs Load Power

8 Parameter Measurement Information

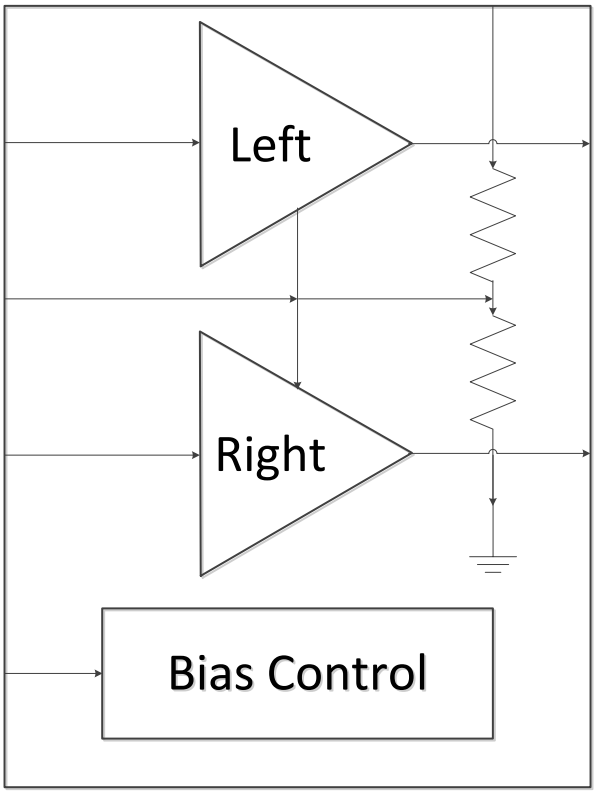
All parameters are measured according to the conditions described in the *Specifications* section.

9 Detailed Description

9.1 Overview

The TPA6111A2 device is a stereo audio power amplifier available in 8-pin SOIC and 8-pin MSOP packages. This device is able to deliver 150 mW of continuous RMS power per channel into 16-Ω loads. The gain of the amplifier is externally configured from 0 dB to 20 dB through two resistors per channel. The TPA6111A2 device is fully specified for operation at 3.3 V and 5 V, which makes this device ideal for PC and mobile applications.

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 5-V Versus 3.3-V Operation

The TPA6111A2 was designed for operation over a supply range of 2.5 V to 5.5 V. This data sheet provides full specifications for 5-V and 3.3-V operation because these are considered to be the two most common standard voltages. There are no special considerations for 3.3-V versus 5-V operation as far as supply bypassing, gain setting, or stability. The most important consideration is that of output power. Each amplifier in the TPA6111A2 can produce a maximum voltage swing of V_{DD} – 1 V. This means, for 3.3-V operation, clipping starts to occur when $V_{O(PP)}$ = 2.3 V as opposed when $V_{O(PP)}$ = 4 V while operating at 5 V. The reduced voltage swing subsequently reduces maximum output power into the load before distortion begins to become significant.

9.4 Device Functional Modes

The TPA6111A2 can be put in shutdown mode when asserting SHUTDOWN pin to a logic HIGH level. While in shutdown mode, the device is turned off, making the current consumption very low. The device exits shutdown mode when a LOW logic level is applied to SHUTDOWN pin.

10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

This typical connection diagram highlights the required external components and system level connections for proper operation of the device in popular use case. Any design variation can be supported by TI through schematic and layout reviews. Visit http://e2e.ti.com for design assistance and join the audio amplifier discussion forum for additional information.

10.2 Typical Application

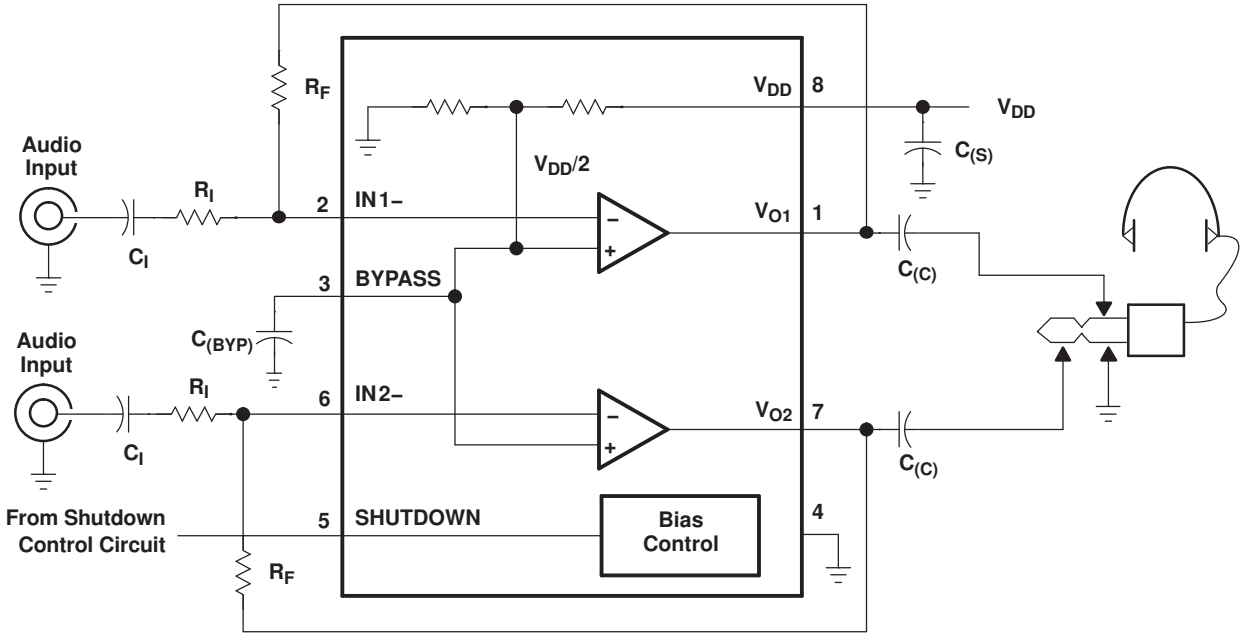


Figure 35. Typical Application

10.2.1 Design Requirements

Table 2 lists the design requirements of the TPA111A2.

Table 2. Design Requirements

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage supply range	3.3 V to 5 V
Current	2 mA
Load impedance	16 Ω

10.2.2 Detailed Design Procedure

10.2.2.1 Gain Setting Resistors, R_F and R_i

The gain for the TPA6111A2 is set by resistors R_F and R_I according to Equation 1.

$$Gain = -\left(\frac{R_F}{R_I}\right) \tag{1}$$

Given that the TPA6111A2 is a MOS amplifier, the input impedance is high. Consequently, input leakage currents are not generally a concern, although noise in the circuit increases as the value of R_F increases. In addition, a certain range of R_F values is required for proper start-up operation of the amplifier. Taken together, TI recommends that the effective impedance seen by the inverting node of the amplifier be set between 5 kΩ and 20 kΩ. The effective impedance is calculated in Equation 2.

$$Effective\ Impedance = -\left(\frac{R_F R_I}{R_F + R_I}\right) \tag{2}$$

As an example, consider an input resistance of 20 kΩ and a feedback resistor of 20 kΩ. The gain of the amplifier would be –1 and the effective impedance at the inverting terminal would be 10 kΩ, which is within the recommended range.

For high-performance applications, metal film resistors are recommended because they tend to have lower noise levels than carbon resistors. For values of R_F above 50 kΩ, the amplifier tends to become unstable due to a pole formed from R_F and the inherent input capacitance of the MOS input structure. For this reason, a small compensation capacitor of approximately 5 pF must be placed in parallel with R_F. In effect, this creates a low-pass filter network with the cutoff frequency defined in Equation 3.

$$f_{c(lowpass)} = \frac{1}{2\pi R_F C_F} \tag{3}$$

For example, if R_F is 100 kΩ and C_F is 5 pF, then $f_{c(lowpass)}$ is 318 kHz, which is well outside the audio range.

10.2.2.2 Input Capacitor, C_i

In the typical application, input capacitor C_I is required to allow the amplifier to bias the input signal to the proper DC level for optimum operation. In this case, C_i and R_I form a high-pass filter with the corner frequency determined in Equation 4.

$$f_{c(highpass)} = \frac{1}{2\pi R_I C_I} \tag{4}$$

The value of C_I is important to consider, as it directly affects the bass (low-frequency) performance of the circuit. Consider the example where R_I is 20 kΩ and the specification calls for a flat bass response down to 20 Hz. Equation 4 is reconfigured as Equation 5.

$$C_I = \frac{1}{2\pi R_I f_{c(highpass)}} \tag{5}$$

In this example, C_I is 0.40 µF, so TI recommends choosing a value in the range of 0.47 µF to 1 µF. A further consideration for this capacitor is the leakage path from the input source through the input network (R_I, C_I) and the feedback resistor (R_F) to the load. This leakage current creates a DC offset voltage at the input to the amplifier that reduces useful headroom, especially in high-gain applications (> 10). For this reason a low-leakage tantalum or ceramic capacitor is the best choice. When polarized capacitors are used, the positive side of the capacitor must face the amplifier input in most applications, as the DC level there is held at $V_{DD}/2$, which is likely higher than the source DC level.

NOTE

It is important to confirm the capacitor polarity in the application.

10.2.2.3 Power Supply Decoupling, $C_{(S)}$

The TPA6111A2 is a high-performance CMOS audio amplifier that requires adequate power supply decoupling to ensure that the output total harmonic distortion (THD) is as low as possible. Power supply decoupling also prevents oscillations for long lead lengths between the amplifier and the speaker. The optimum decoupling is achieved by using two capacitors of different types that target different types of noise on the power supply leads. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance (ESR) ceramic capacitor, typically 0.1 µF, placed as close as possible to the device V_{DD} lead, works best. For filtering lower frequency noise signals, a larger aluminum electrolytic capacitor of 10 µF or greater placed near the power amplifier is recommended.

10.2.2.4 Midrail Bypass Capacitor, $C_{(BYP)}$

The midrail bypass capacitor, $C_{(BYP)}$, serves several important functions. During start-up, $C_{(BYP)}$ determines the rate at which the amplifier starts up. This helps to push the start-up pop noise into the subaudible range (so low it cannot be heard). The second function is to reduce noise produced by the power supply caused by coupling into the output drive signal. This noise is from the midrail generation circuit internal to the amplifier. The capacitor is fed from a 230-kΩ source inside the amplifier. To keep the start-up pop as low as possible, the relationship shown in Equation 6 must be maintained.

$$\frac{1}{\left(C_{(BYP)} \times 230\ k\Omega\right)} \leq \frac{1}{(C_I R_I)} \tag{6}$$

As an example, consider a circuit where $C_{(BYP)}$ is 1 µF, C_I is 1 µF, and R_I is 20 kΩ. Inserting these values into Equation 6 results in: 6.25 ≤ 50 which satisfies the rule. Recommended values for bypass capacitor $C_{(BYP)}$ are 0.1-µF to 1-µF, ceramic or tantalum low-ESR, for the best THD and noise performance.

10.2.2.5 Output Coupling Capacitor, $C_{(C)}$

In the typical single-supply single-ended (SE) configuration, an output coupling capacitor (C_C) is required to block the DC bias at the output of the amplifier, thus preventing DC currents in the load. As with the input coupling capacitor, the output coupling capacitor and impedance of the load form a high-pass filter governed by Equation 7.

$$f_c = \frac{1}{2\pi R_L C_{(C)}} \tag{7}$$

The main disadvantage, from a performance standpoint, is that the typically small load impedances drive the low-frequency corner higher. Large values of $C_{(C)}$ are required to pass low frequencies into the load. Consider the example where a $C_{(C)}$ of 68 µF is chosen and loads vary from 32 Ω to 47 kΩ. Table 3 summarizes the frequency response characteristics of each configuration.

Table 3. Common Load Impedances vs Low Frequency Output Characteristics in SE Mode

R_L	C_C	LOWEST FREQUENCY
32 Ω	68 µF	73 Hz
10,000 Ω	68 µF	0.23 Hz
47,000 Ω	68 µF	0.05 Hz

As Table 3 indicates, headphone response is adequate and drive into line level inputs (a home stereo for example) is good.

The output coupling capacitor required in single-supply SE mode also places additional constraints on the selection of other components in the amplifier circuit. With the rules described earlier still valid, add the following relationship in Equation 8:

$$\frac{1}{\left(C_{(BYP)} \times 230\ k\Omega\right)} \leq \frac{1}{(C_I R_I)} \leq \frac{1}{R_L C_{(C)}} \tag{8}$$

10.2.2.6 Using Low-ESR Capacitors

Low-ESR capacitors are recommended throughout this application. A real capacitor can be modeled simply as a resistor in series with an ideal capacitor. The voltage drop across this resistor minimizes the beneficial effects of the capacitor in the circuit. The lower the equivalent value of this resistance, the more the real capacitor behaves like an ideal capacitor.

10.2.3 Application Curves

The characteristics of this design are shown in Table 4 from the *Typical Characteristics* section.

Table 4. Table of Graphs

		FIGURE
THD+N Total harmonic distortion plus noise	vs Frequency	Figure 11
	vs Output power	Figure 12

11 Power Supply Recommendations

The device is designed to operate form an input voltage supply of 3.3 V and 5 V. Therefore, the output voltage range of power supply must be within this range and well regulated. Ti recommends placing decoupling capacitors in every voltage source pin. Place these decoupling capacitors as close as possible to the TPA6111A2.

12 Layout

12.1 Layout Guidelines

Solder the exposed metal pad on the TPA6111A2 DGN package to the PCB. The pad on the PCB may be grounded or may be allowed to float (not be connected to ground or power). If the pad is grounded, it must be connected to the same ground as the GND pin (4). See the layout and mechanical drawings in *Mechanical, Packaging, and Orderable Information* for proper sizing. Soldering the thermal pad improves mechanical reliability, improves grounding of the device, and enhances thermal conductivity of the package.

12.2 Layout Examples

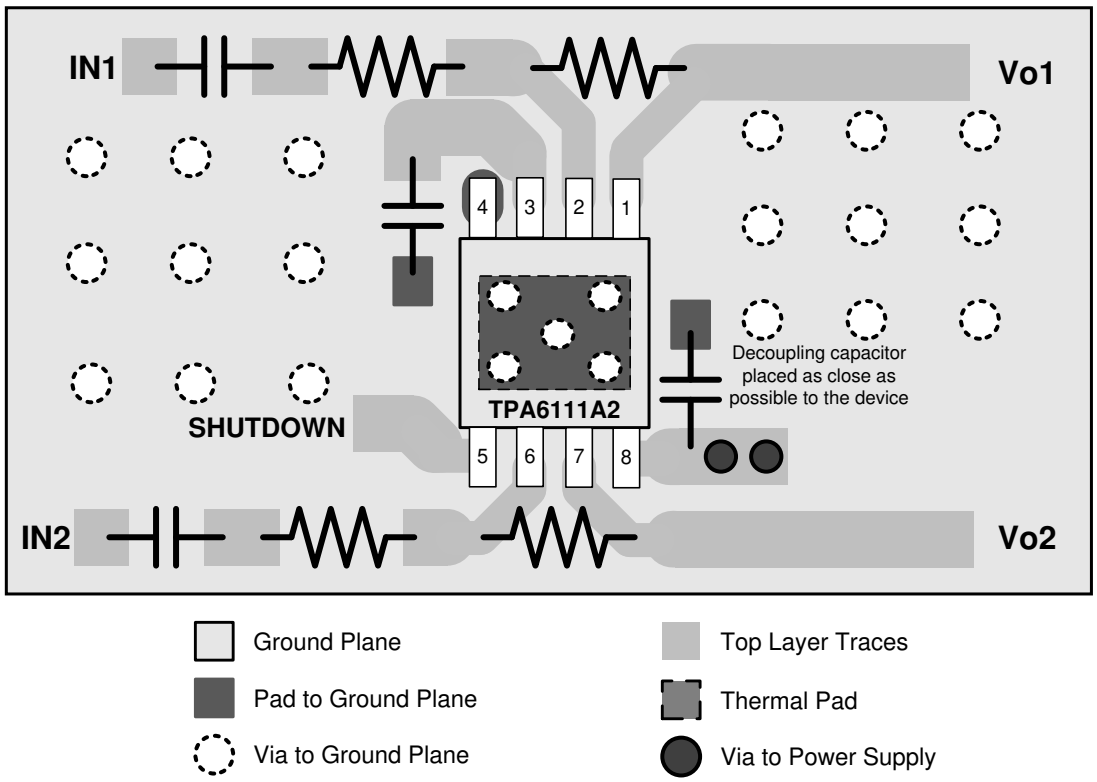


Figure 36. TPA611A2 MSOP Layout Example

Layout Examples (continued)

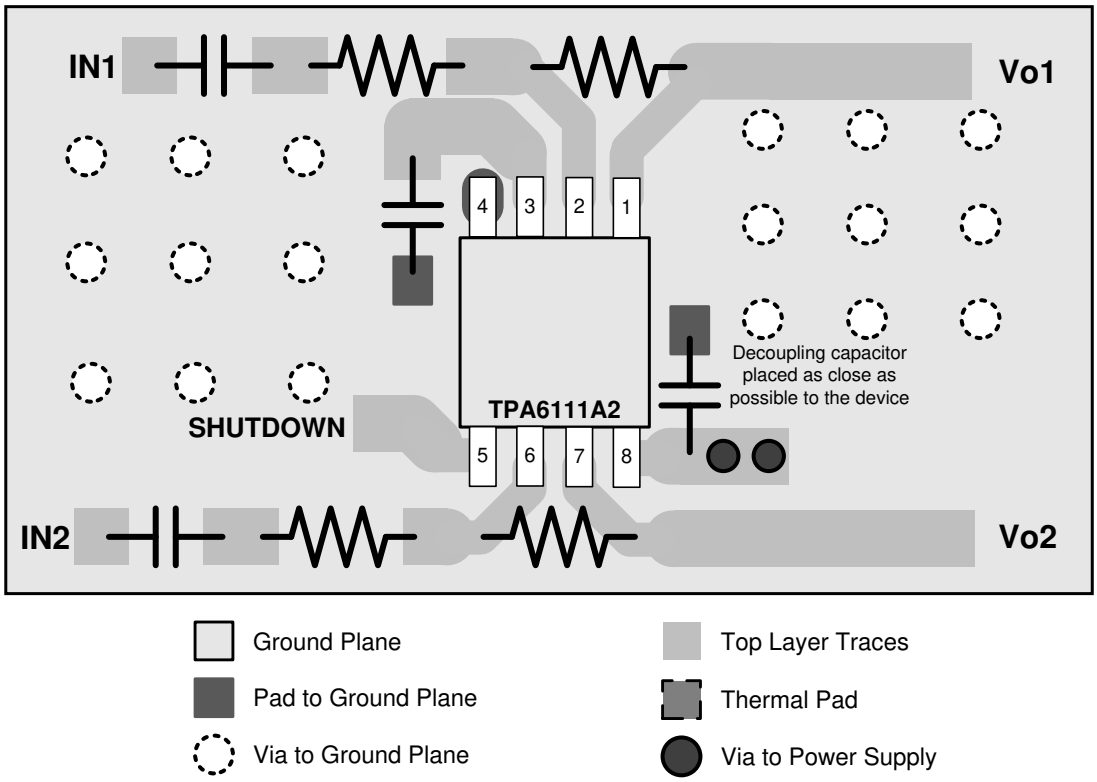


Figure 37. TPA611A2 SOIC Layout Example

13 Device and Documentation Support

13.1 Documentation Support

13.1.1 Related Documentation

For related documentation, see the following:

PowerPAD Thermally Enhanced Package Application Report (SLMA002)

13.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

13.3 Trademarks

PowerPAD, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

13.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
HPA00577DGNR	ACTIVE	MSOP-PowerPAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	AJA	Samples
TPA6111A2D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	6111A2	Samples
TPA6111A2DGN	ACTIVE	MSOP-PowerPAD	DGN	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	AJA	Samples
TPA6111A2DGNG4	ACTIVE	MSOP-PowerPAD	DGN	8	80	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	AJA	Samples
TPA6111A2DGNR	ACTIVE	MSOP-PowerPAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	AJA	Samples
TPA6111A2DGNRG4	ACTIVE	MSOP-PowerPAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	AJA	Samples
TPA6111A2DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	6111A2	Samples
TPA6111A2DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	6111A2	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

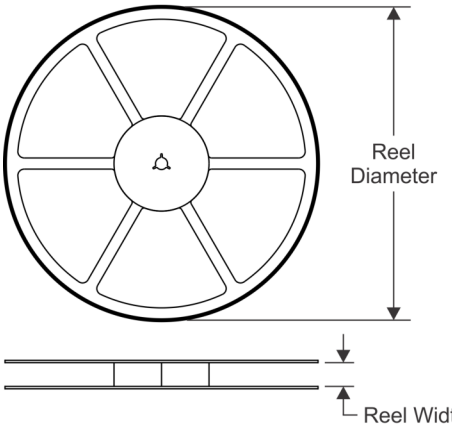
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

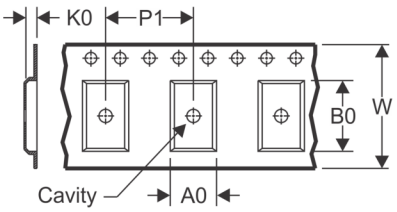
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

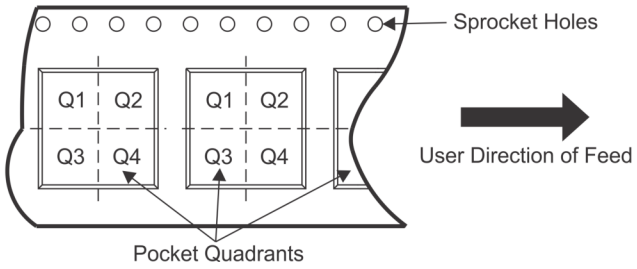


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

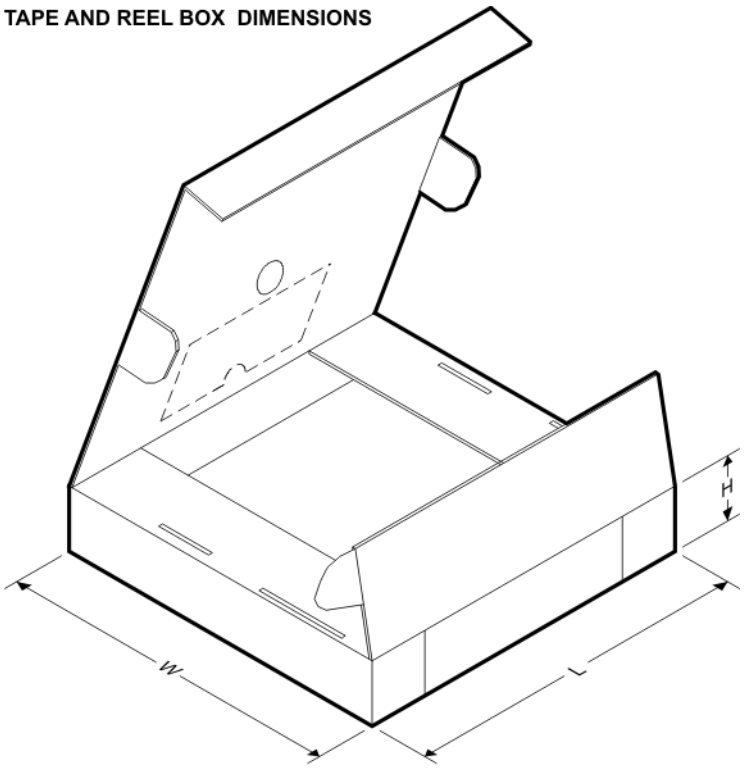
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPA6111A2DGNR	MSOP-Power PAD	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPA6111A2DGNR	MSOP-Power PAD	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPA6111A2DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

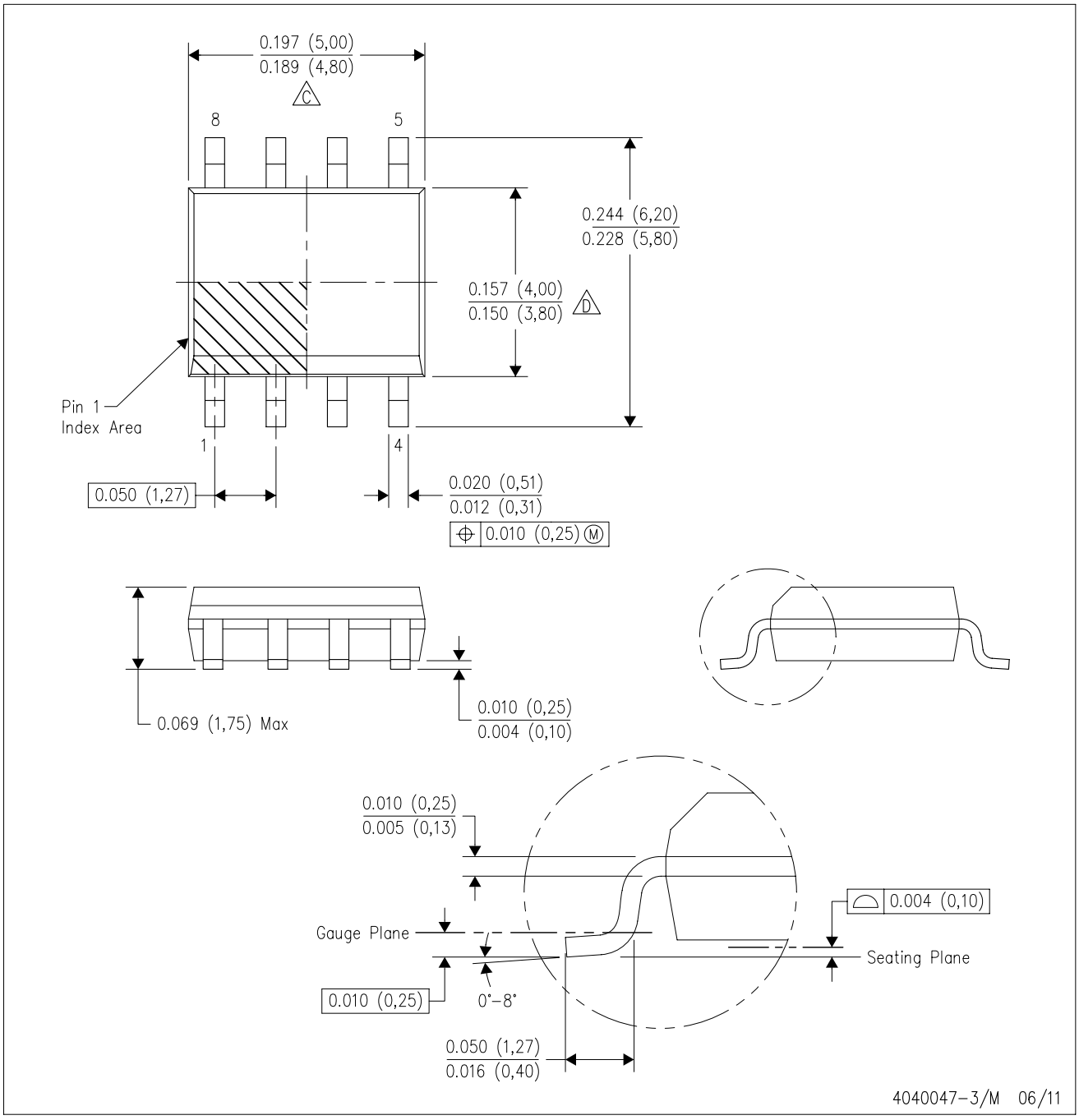
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

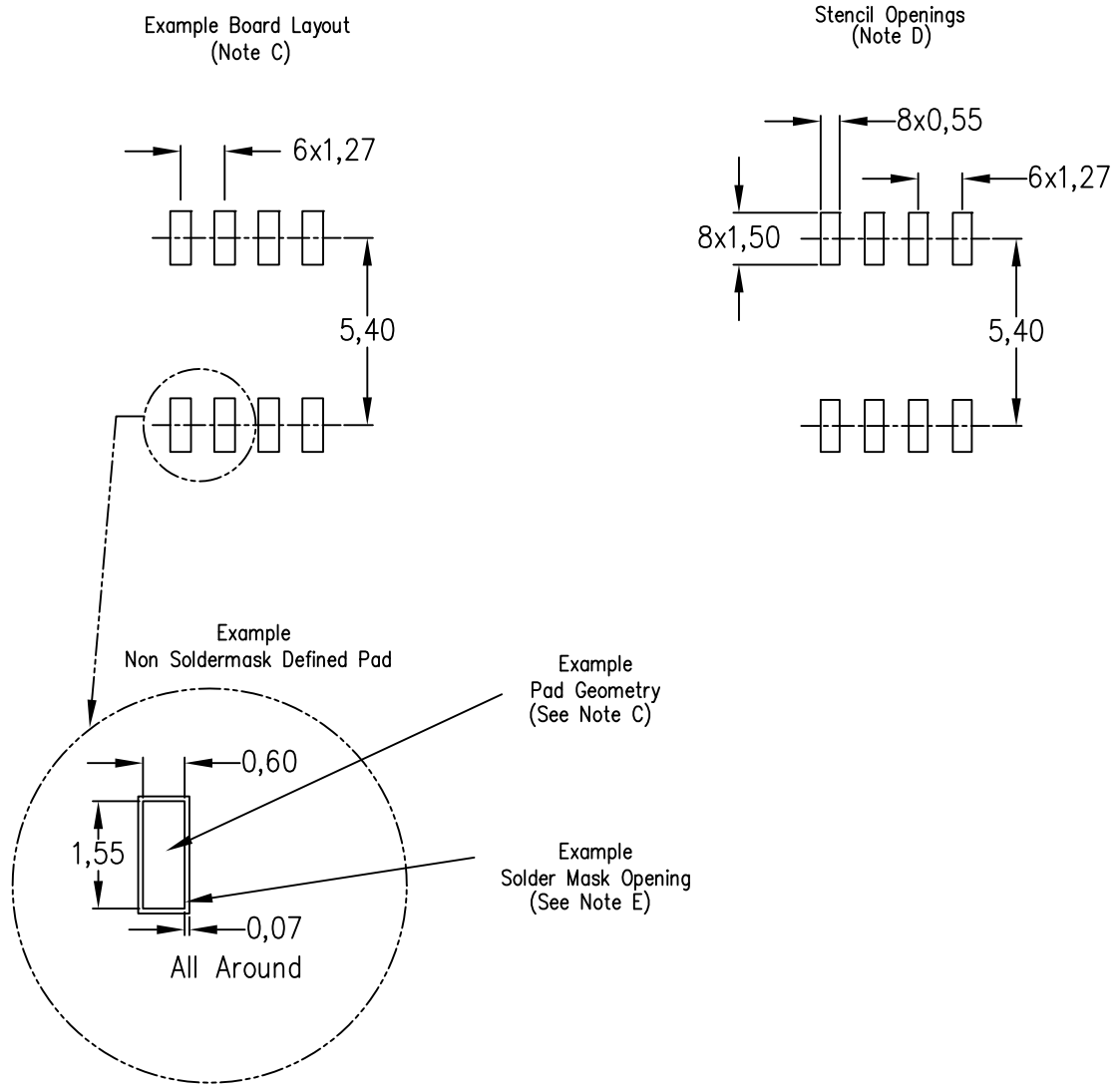
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPA6111A2DGNR	MSOP-PowerPAD	DGN	8	2500	364.0	364.0	27.0
TPA6111A2DGNR	MSOP-PowerPAD	DGN	8	2500	358.0	335.0	35.0
TPA6111A2DR	SOIC	D	8	2500	340.5	338.1	20.6

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



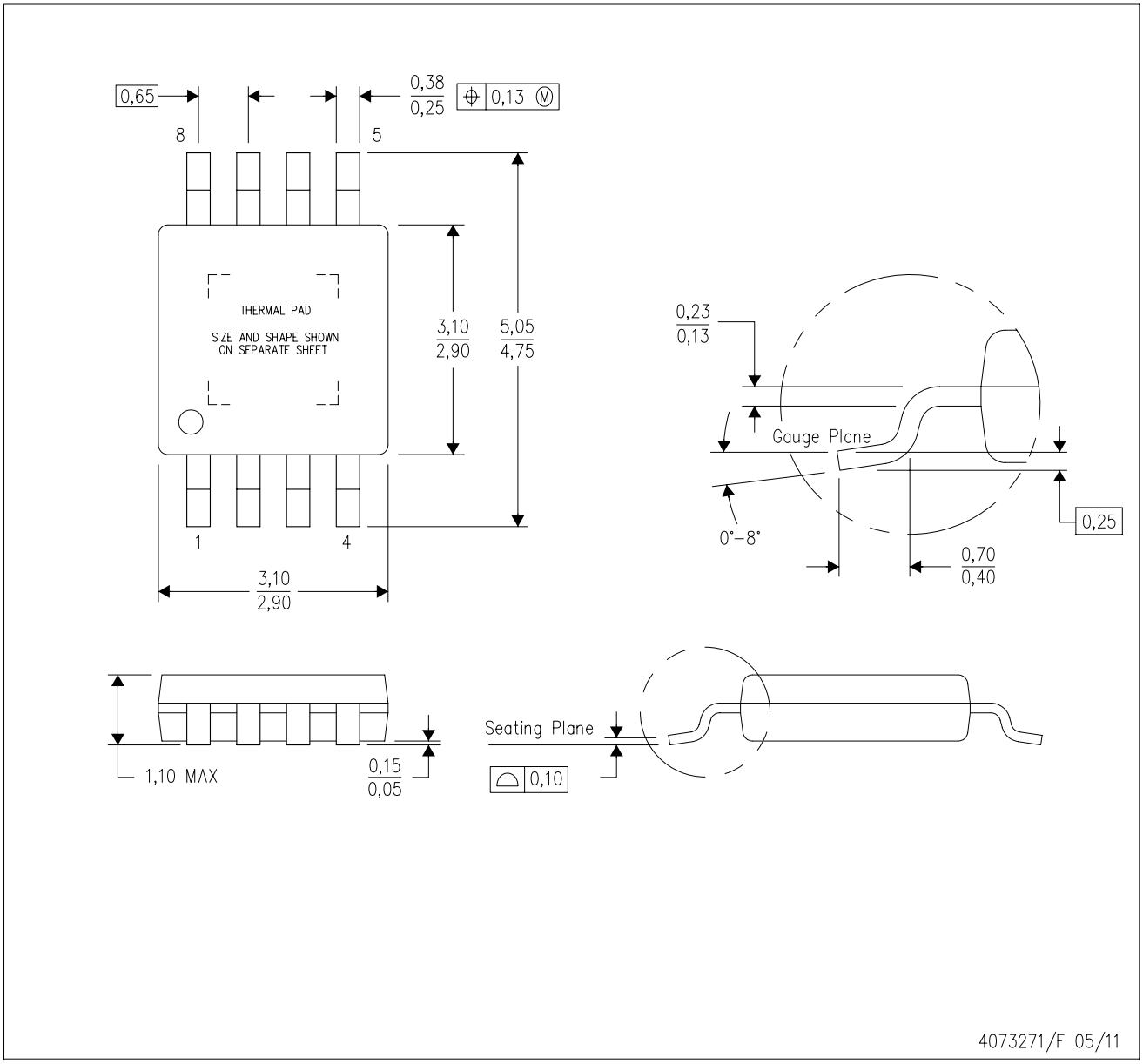
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DGN (S–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–187 variation AA–T

PowerPAD is a trademark of Texas Instruments.

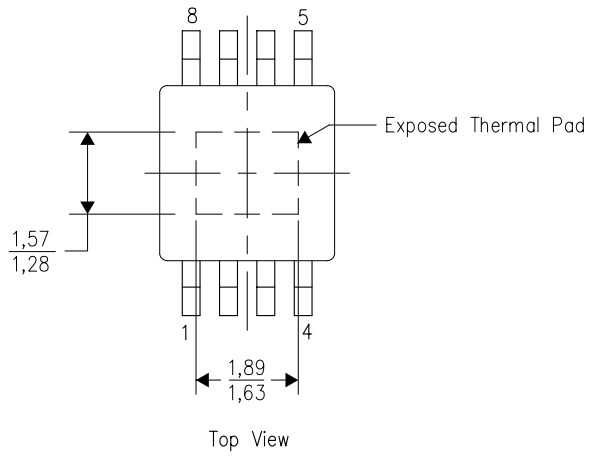
DGN (S–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

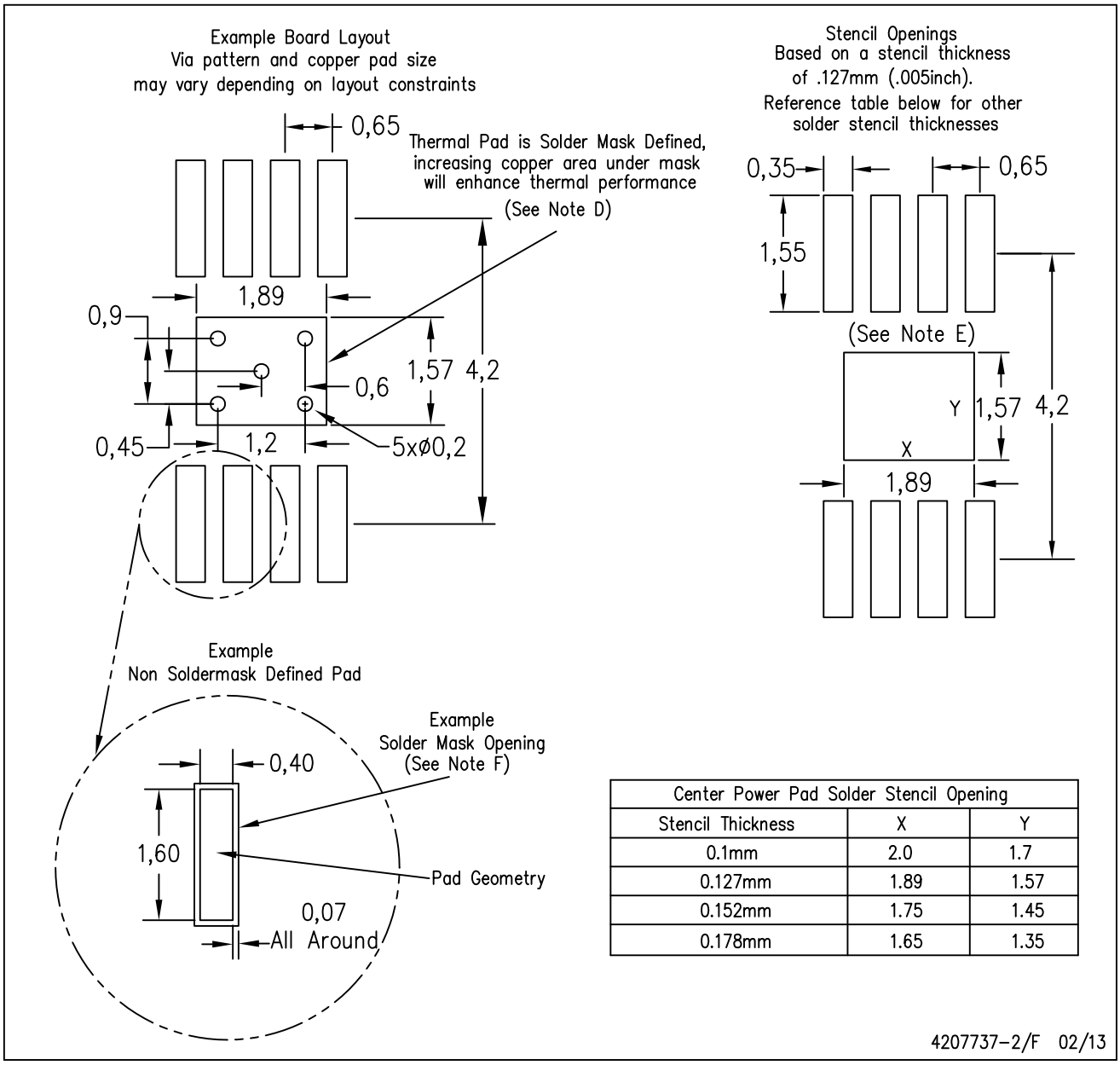
Exposed Thermal Pad Dimensions

4206323–2/I 12/11

NOTE: All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments

DGN (R–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	2.0	1.7
0.127mm	1.89	1.57
0.152mm	1.75	1.45
0.178mm	1.65	1.35

4207737–2/F 02/13

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

IMPORTANT NOTICE

Texas Instruments Incorporated (TI) reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete.

TI's published terms of sale for semiconductor products (http://www.ti.com/sc/docs/stdterms.htm) apply to the sale of packaged integrated circuit products that TI has qualified and released to market. Additional terms may apply to the use or sale of other types of TI products and services.

Reproduction of significant portions of TI information in TI data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such reproduced documentation. Information of third parties may be subject to additional restrictions. Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyers and others who are developing systems that incorporate TI products (collectively, "Designers") understand and agree that Designers remain responsible for using their independent analysis, evaluation and judgment in designing their applications and that Designers have full and exclusive responsibility to assure the safety of Designers' applications and compliance of their applications (and of all TI products used in or for Designers' applications) with all applicable regulations, laws and other applicable requirements. Designer represents that, with respect to their applications, Designer has all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. Designer agrees that prior to using or distributing any applications that include TI products, Designer will thoroughly test such applications and the functionality of such TI products as used in such applications.

TI's provision of technical, application or other design advice, quality characterization, reliability data or other services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using TI Resources in any way, Designer (individually or, if Designer is acting on behalf of a company, Designer's company) agrees to use any particular TI Resource solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

Designer is authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY DESIGNER AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

Unless TI has explicitly designated an individual product as meeting the requirements of a particular industry standard (e.g., ISO/TS 16949 and ISO 26262), TI is not responsible for any failure to meet such industry standard requirements.

Where TI specifically promotes products as facilitating functional safety or as compliant with industry functional safety standards, such products are intended to help enable customers to design and create their own applications that meet applicable functional safety standards and requirements. Using products in an application does not by itself establish any safety features in the application. Designers must ensure compliance with safety-related requirements and standards applicable to their applications. Designer may not use any TI products in life-critical medical equipment unless authorized officers of the parties have executed a special contract specifically governing such use. Life-critical medical equipment is medical equipment where failure of such equipment would cause serious bodily injury or death (e.g., life support, pacemakers, defibrillators, heart pumps, neurostimulators, and implantables). Such equipment includes, without limitation, all medical devices identified by the U.S. Food and Drug Administration as Class III devices and equivalent classifications outside the U.S.

TI may expressly designate certain products as completing a particular qualification (e.g., Q100, Military Grade, or Enhanced Product). Designers agree that it has the necessary expertise to select the product with the appropriate qualification designation for their applications and that proper product selection is at Designers' own risk. Designers are solely responsible for compliance with all legal and regulatory requirements in connection with such selection.

Designer will fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of Designer's non-compliance with the terms and provisions of this Notice.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265